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World Bulletin of Education and Learning (WBEL)

ISSN (E): 3072-175X | Volume 2, Issue 5, May 2026

https://worldbulletin.org/index.php/1

DEVELOPMENT AND RESEARCH OF A T- AND D-TRIGGERS BASED ON COMPLEMENTARY BIPOLAR TRANSISTORS

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Abstract

The study proposed T- and D-type flip-flop circuits based on complementary bipolar transistors. Mathematical modeling and simulation in PROTEUS confirmed the feasibility of achieving high switching speeds corresponding to frequencies up to 1 GHz. Reviewing the basic transistor designs and operating characteristics enabled the development of a structure that balances operating speed and energy efficiency. The theoretical foundations laid out at the beginning of the article and their practical implementation at the end ensured the correctness of the developed solution, which meets the stated research objectives.

The timing characteristics of the proposed triggers demonstrated their significant advantages. Improved dynamic parameters, such as recovery time and switching delays, ensure high performance. Energy efficiency in static modes further confirms the architecture's potential for use in sequential circuits. The analysis results presented at the end of the article revealed the superiority of the developed triggers in key metrics. This makes it suitable for use in highly loaded devices where the combination of speed and low power consumption is critical. These recommendations pave the way for further research into increasing the level of integration and adapting technology to modern microelectronic systems. This is in line with the relevance of the work related to energy efficiency and performance requirements.

Therefore, this article is of significant importance for the further development of information storage technologies and the optimization of modern electronic devices.

Keywords: Complementary bipolar transistor, T-trigger, D-trigger, sequential digital circuits.

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ISSN (E): 3072-175X | Volume 2, Issue 5, May 2026

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Introduction

KOMPLEMENTAR BIPOLYAR TRANZISTORLARGA ASOSLANGAN T- VA D-TRIGGERLARINI ISHLAB CHIQISH VA TADQIQ ETISH

Annotatsiya

Tadqiqotda komplementar bipolyar tranzistorlarga asoslangan T- va D-trigger sxemalari taklif qilindi. PROTEUSda matematik modellashtirish va simulyatsiya 1 gigagertsgacha bo'lgan chastotalarga mos keladigan yuqori kommutatsiya tezligiga erishish mumkinligini tasdiqladi. Asosiy tranzistor dizaynlari va ish xususiyatlarini ko'rib chiqish ish tezligi va energiya samaradorligini muvozanatlashtiradigan tuzilmani ishlab chiqish imkonini berdi. Maqolaning boshida qo'yilgan nazariy asoslar va oxirida ularni amaliy qo'llash belgilangan tadqiqot maqsadlariga javob beradigan ishlab chiqilgan yechimning to'g'riligini ta'minladi.

Taklif qilingan triggerlarning vaqt diagrammalari ularning muhim afzalliklarini namoyish etdi. Qayta tiklash vaqti va kommutatsiya kechikishlari kabi yaxshilangan dinamik parametrlar yuqori ishlashni ta'minlaydi. Statik rejimlarda energiya samaradorligi arxitekturaning ketma-ket sxemalarda foydalanish potentsialini yanada tasdiqlaydi. Maqola oxirida taqdim etilgan tahlil natijalari ishlab chiqilgan triggerlarning asosiy ko'rsatkichlardagi ustunligini ochib berdi. Bu uni tezlik va kam quvvat sarfi kombinatsiyasi juda muhim bo'lgan yuqori yuklangan qurilmalarda foydalanish uchun moslashtiradi. Ushbu tavsiyalar integratsiya darajasini oshirish va texnologiyani zamonaviy mikroelektron tizimlarga moslashtirish bo'yicha keyingi tadqiqotlar uchun yo'l ochadi. Bu energiya samaradorligi va ishlash talablari bilan bog'liq ishning dolzarbligiga mos keladi.

Shuning uchun ushbu maqola axborotni saqlash texnologiyalarini yanada rivojlantirish va zamonaviy elektron qurilmalarni optimallashtirish uchun katta ahamiyatga ega.

Ushbu tadqiqot ketma-ketli qurilmalarni tuzish uchun asos bo'lgan komplementar bipolyar tranzistorlarga asoslangan T- va D-trigger sxemalarini ishlab chiqish va modellashtirishga ba'gishlangan. Ularning ishlash tamoyillari

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va vaqt diagrammalari batafsil tahlil qilingan va tizimlashtirilgan. Taklif qilingan sxema konstruksiyalaridan foydalanib, taxminan 0,7 V past kuchlanishli integral sxemalar uchun yangi konstruksiya variantlarini taklif qilish mumkin.

Kalit so‘zlar: komplementar bipolyar tranzistor, T-trigger, D-trigger, ketma-ketli raqamli sxemalar.

РАЗРАБОТКА И ИССЛЕДОВАНИЕ Т- И D-ТРИГГЕРОВ НА ОСНОВЕ КОМПЛЕМЕНТАРНЫХ БИПОЛЯРНЫХ ТРАНЗИСТОРОВ

Аннотация

В ходе исследования были предложены схемы Т- и Д- на основе комплементарных биполярных транзисторов. Математическое моделирование и симуляция в PROTEUS подтвердили возможность достижения высокой скорости переключения, соответствующей частотам до 1 ГГц. Просмотр основных чертежей и рабочих характеристик транзисторов дал возможность разработать структуру, показывающую баланс между скоростью работы и эффективностью потребления энергии. Теоретические основы заложенные в начале статьи и практическая реализация их в конце обеспечили корректность разработанного решения, отвечающего поставленной цели исследования.

Временные характеристики предложенных триггеров показали их существенные преимущества. Улучшенные динамические параметры, такие как время восстановления и задержки переключения, обеспечивают высокую производительность. Энергоэффективность в статических режимах дополнительно подтверждает перспективность архитектуры для применения в последовательностных цепях. Результаты анализа, представленные в конце статьи, выявили превосходство разработанных триггеров по ключевым метрикам. Это делает её пригодной для использования в высоконагруженных устройствах, где сочетание скорости и низкого энергопотребления является критически важным фактором.

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Данные рекомендации открывают пути для дальнейших исследований в области повышения уровня интеграции и адаптации технологии к современным микроэлектронным системам. Это соответствует актуальности работы, связанной с требованиями к энергоэффективности и производительности.

Таким образом, статья имеет значительное значение для дальнейшего развития технологий хранения информации и оптимизации работы современных электронных устройств.

Ключевые слова: комплементарный биполярный транзистор, Т-триггер, D-триггер, последовательные цифровые схемы.

Introduction

Design methods for digital devices that perform complex logic functions depend on the type of logic cell used. The simplest cell is an inverter based on complementary bipolar transistors (CBTs).

CBTs are a combination of n-p-n and p-n-p structures integrated on a single substrate. Their operation is based on the principle of controlling collector current by varying base current. For n-p-n transistors, this is achieved by applying a positive voltage to the base relative to the emitter, which leads to the injection of electrons from the emitter into the base and their subsequent drift to the collector. Similarly, p-n-p transistors operate when a negative voltage is applied to the base relative to the emitter, ensuring hole movement. The interaction of these two types of transistors allows for the creation of complex logic circuits with improved characteristics. For example, in complementary circuits, one transistor can act as an active load for the other, facilitating more efficient switching. This fundamental property provides the basis for constructing inverters, electronic switches, and other basic elements of digital electronics, which is critical for the implementation of sequential digital devices [1, 2].

The key advantages of CBTs over traditional solutions are their high energy efficiency and high speed. These characteristics are achieved through the use of a complementary structure, which minimizes static currents when quiescent. At

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ISSN (E): 3072-175X
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the same time, high switching speed is ensured by efficient charge management in the transistor base, reducing signal propagation delays [3].

Research

The main challenges in triggers design relate to state instability, timing constraints, prohibited input combinations, and sensitivity to noise. Key challenges include the risk of unpredictable behavior when signals are applied simultaneously, switching delays, and issues of integrated circuit degradation under load.

The main technical problems of triggers design are: forbidden states (RS-trigger), asynchronous delays, contact bounce, synchronization problems, degradation under load, sensitivity to interference.

D-trigger. If we take a synchronous RS-trigger and apply a signal directly to the S input and through an inverter to the R input, we get an element that delays the input signal until the next high clock pulse. This is called a D- trigger, short for "delay." Essentially, it has no set or reset inputs; instead, it has a single data input, D.

The truth table of a D- trigger is very simple – thanks to the inverter between the reset and set inputs, there is no forbidden state for the circuit.

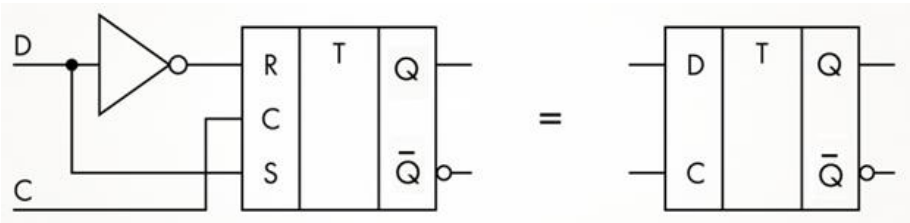

Fig. 1. Schematic and symbol of a D-trigger

Truth table of D-trigger

C	D	$Q(t)$	$\bar{Q}(t)$	Operating mode
0	X	$Q(t-1)$	$\bar{Q}(t-1)$	Storage
1	0	0	1	Transfer of zero
1	1	1	0	Transfer of unit

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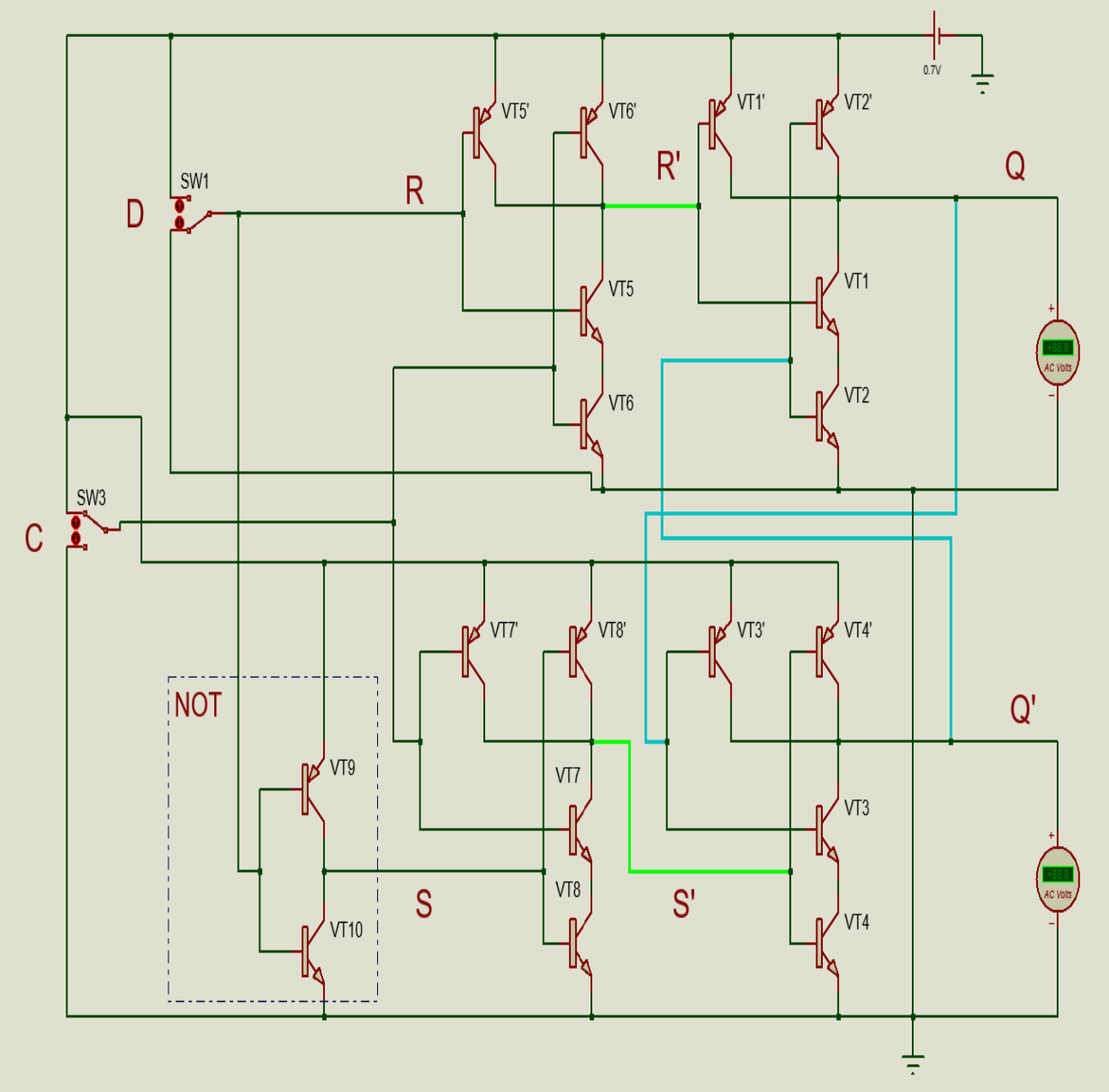

Fig. 2. Results of a virtual study of the operation of a D-trigger assembled on a CBT

It's easy to guess that a two-stage RS-trigger can easily be converted into a two-stage D flip-flop by adding just one inverter. Such D- triggers form the basis of the data flow control system in microprocessors and microcontrollers, which regulate the flow of zeros and ones across the chip. After all, the chip is very

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large in terms of the number of devices it contains and the bits flowing through the wires from device to device.

The timing diagram of the D-trigger is not very complicated after the previously studied synchronous RS-triggers (Fig. 3)

To prevent chaos, data is periodically paused on D-triggers and awaits a command to advance to the next flip-flop. Multi-bit data, for example, 32-bit data, is fed to the inputs of 32 triggers simultaneously, controlled by a common clock signal.

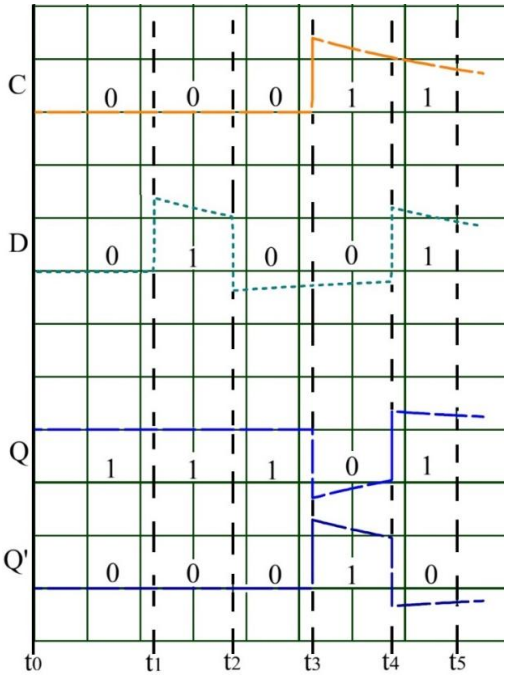

Fig. 3. Fragment of the timing diagram of the D-trigger operation

T-trigger based on 2AND-NOT LE (two-stage). The advantage of level-activated triggers is their simplicity. However, for correct operation, the input signal must be held constant during the time interval during which the clock signal is at an active level.

In electronics, there are generally accepted names for the different parts of a digital signal's timing diagram. These are the high logic level (one) and the low logic level (zero). The signal transition from zero to one is called a pulse rise,

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and from one to zero, a transition. These sections are drawn vertically on the timing diagram.

To force circuits to switch precisely on these sections of the clock signal, two-stage trigger circuits are used. These are called **master-slave**, or **MS-triggers**.

When the clock signal is high, the first "master" trigger can accept commands from the R and S inputs and transmit them to its outputs – the wires labeled U and D in the diagram above. Meanwhile, the second "slave" trigger is in storage mode, ignoring the state of its U and D inputs. When the clock signal transitions from one to zero, the master trigger stops responding to changes in input levels until the next rising edge. The slave trigger, on the other hand, begins to receive information from the master's outputs and switches to a new state.

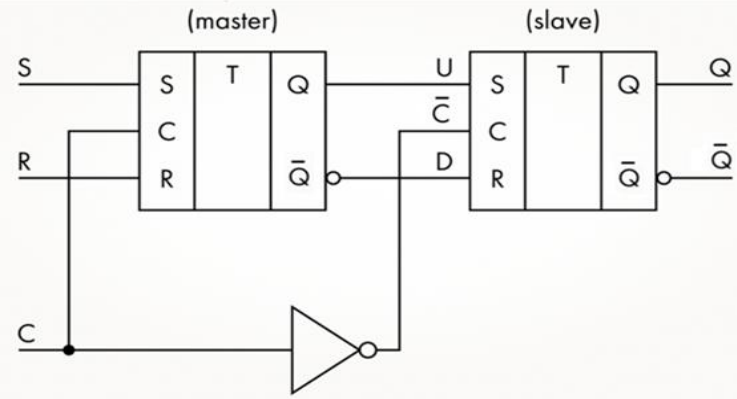

Fig. 4. T-trigger (two-stage)

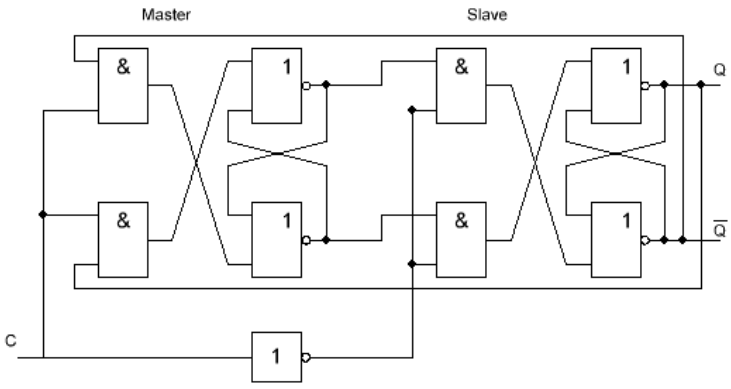

Fig. 5. Logical diagram of the T-trigger implementation

If the data at the MS-trigger inputs changed while C was high, this was not reflected in the Q and $\bar{Q}$ outputs of the entire trigger. Only the state of the S and R inputs – the last state before the clock signal's edge – was significant. After C's edge, during its low level, the input data could change arbitrarily, since the

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master trigger is in hold mode, preventing any switching at the slave's inputs, even though it is transparent at this time (Fig.5).

Asynchronous T-trigger. An asynchronous T-trigger does not have a T-trigger enable input, so the trigger switches to the opposite state when the logic level at the C input changes (Fig.6).

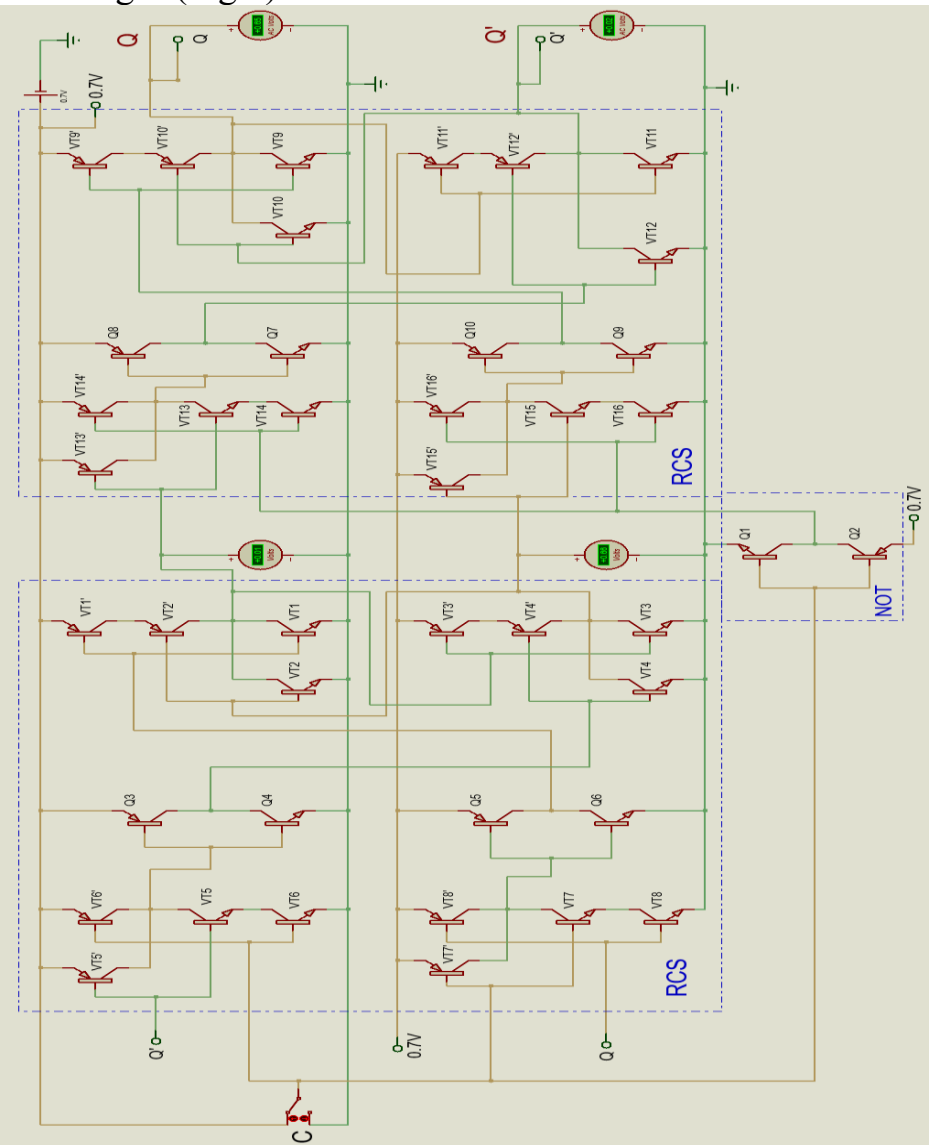

Fig. 6. Results of a virtual study of the operation of a T-trigger assembled on a CBT

In the "pure" asynchronous form, creating a stable T-trigger using simple logic elements (AND-NOT, OR-NOT) is extremely difficult due to the risk of self-oscillation if the input pulse is too long.

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The circuit can be built using a D-trigger, connecting its inverted output to the input. In this case, each change in the signal at the clock input will cause the trigger to "latch" to its inverted value (Fig. 7).

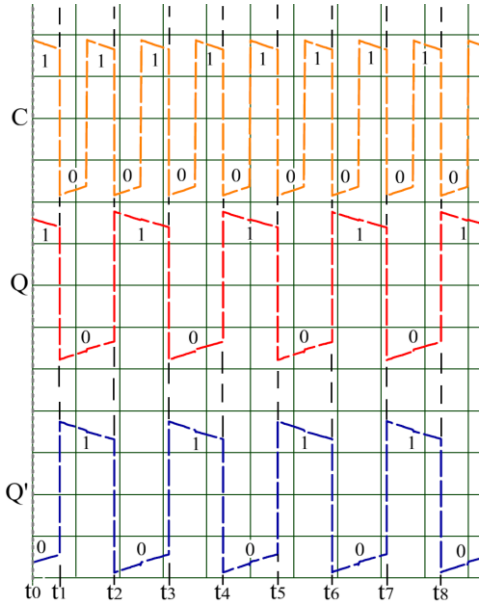

Fig. 7. Fragment of the timing diagram of a two-stage T-trigger

To obtain a reliable T-trigger, it is necessary either to use an additional memory element that stores new values of the R, S or D signals and feeds them to the information inputs of the main memory element only after the active signal is removed from the T input, or to artificially limit the duration of the T signal.

Synchronous T-Trigger. This synchronous trigger has a count enable input. The operating logic is as follows. When the T input is at a logic high, each pulse at the C input causes the trigger to change its state to the opposite. When the T input is at a logic low, signals at the C input are ignored (Fig. 8).

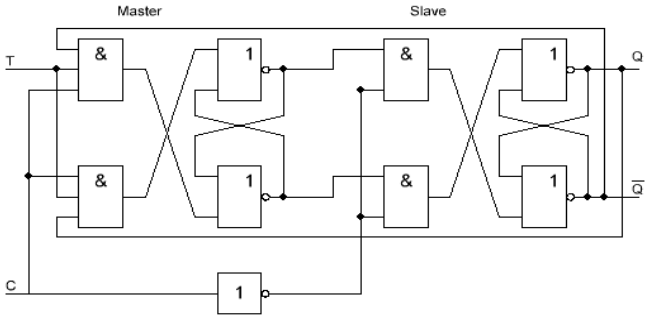

Fig. 8. Logic diagram of a T-trigger implementation, with a count enable input

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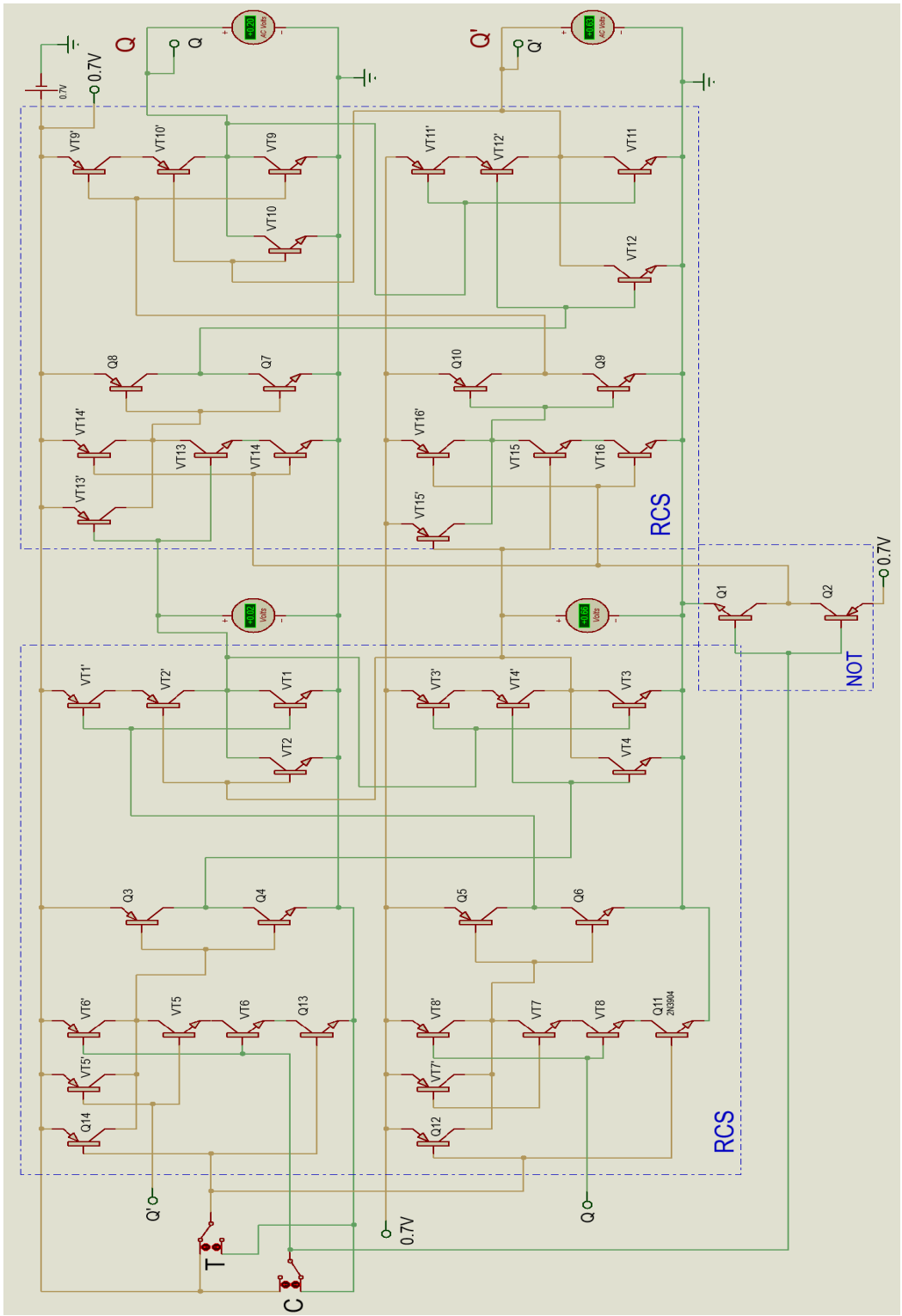

Fig. 9. Results of a virtual study of the operation of a T-trigger with a count enable input

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New information is initially generated only in the input stage of the trigger, while the old information is stored in its output stage. Once the new state of the input stage is generated and the active signal level is removed from the T input, it is overwritten in the output stage of the device.

A synchronous T-trigger does not operate due to the absence of an active signal at the synchronization input (C), as it triggers only on the edge/level of the clock pulse, and not simply on the presence of a logical "1" at the T input (see Fig.10).

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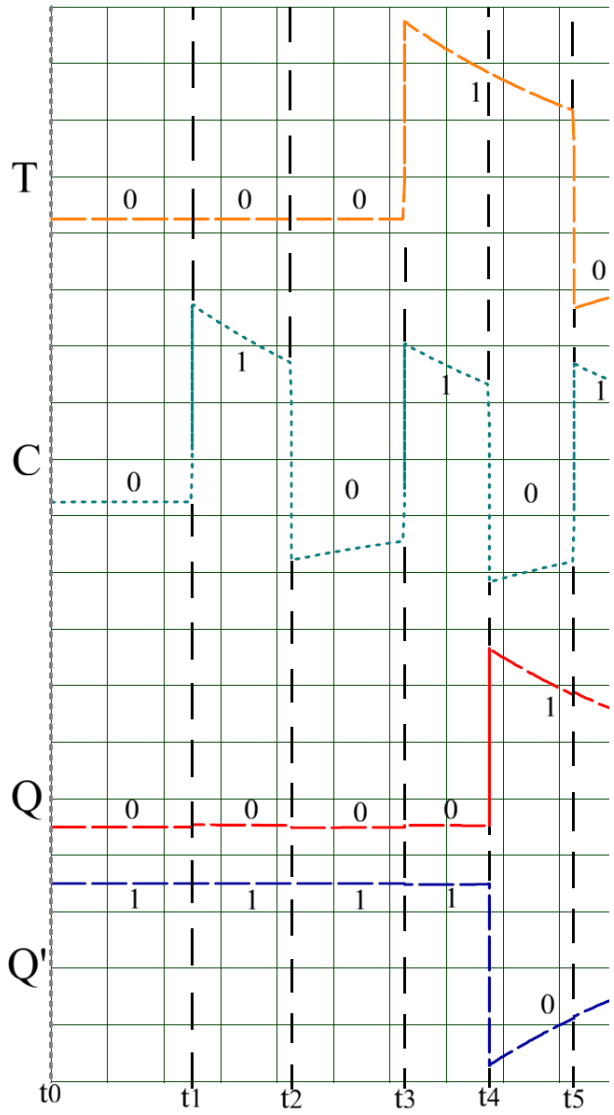

Fig. 10. Fragment of the timing diagram of a two-stage T-trigger

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It turns out that the time window for input data to reach the output is a very narrow, practically limited moment when the clock pulse switches from one state to another. And no special short signals had to be created for synchronization.
In real life, ideal rectangular pulses do not exist – the rise and fall times are always non-zero. But they are so short compared to the stable states of the clock signal that two-stage triggers operate without failure.

Conclusion

The developed T- and D-triggers are the core component of complex triggers. Using the proposed circuit implementations, one can build functional units of digital sequential devices, in particular, registers and frequency dividers.
These research results open avenues for further research into increasing the level of integration and adapting the technology to modern microelectronic systems. This is in line with the relevance of the work related to energy efficiency and performance requirements.

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ISSN (E): 3072-175X | **Volume 2, Issue 5, May 2026**

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